

A CMOS Digital Phase-Locked Loop for Nanometer-Scale Technology

Ping-Hsuan Hsieh

Thesis advisor Professor Chih-Kong Ken Yang

Abstract

Digital implementations of phase-locked loops (DPLLs) have emerged as an attractive alternative as variability and poor analog characteristics of devices plague designs in nanometer CMOS process. With fully-digital loop filters, designs can be portable and easily programmable for operation across a wide range of operating frequencies and process corners, while the design of the digital-controlled oscillator (DCO) and the phase detector (PD) dictates the signal quality and usually remains relatively analog-intensive and challenging.

We propose a DPLL design for clock generation in large digital systems. A 9-bit interpolator-based DCO is used in the proposed design for low jitter performance and wide operating frequency range. The use of an integer divider in the loop filter greatly relaxes the trade-off between the steady-state dithering jitter and the resolution requirement on the DCO. The phase selection is based on a token-passing technique with an asynchronous control block using self-reset circuits to speed up the operation and to reach GHz of operation. With the ability to dynamically sweep the output frequency from 3.5MHz to 1.8GHz, the proposed design is suitable for Dynamic Voltage and Frequency Scaling (DVFS) and spread-spectrum I/O applications. Bandwidth-tracking ability is achieved with the use of replica delay line in the time-to-digital converter (TDC) as the PD. The resulting loop characteristic depends only on the implementation of the digital loop filter. Without calibration, the empirical results show a near constant damping factor and a bandwidth that tracks with input frequency over $2\times$ of core oscillation frequencies (2.5GHz–5.0GHz) and reference frequencies from 19.5MHz to 312MHz. Nonlinear PD transfer curve enables low jitter and fast loop response with fewer TDC levels.

The prototype is designed and implemented with 65nm CMOS technology with the core area of $800\times 700\mu\text{m}^2$. The design consumes 220mW at 1.6GHz with the measured rms/pp jitter of 2.63/22.2ps.

Biography

Ping-Hsuan Hsieh is currently a Ph.D. candidate in the University of California, Los Angeles, working in High-Performance Mixed-Mode Circuit Design with Professor Chih-Kong Ken Yang. She received her B.S. degree in electrical engineering from National Taiwan University in 2001, and the M.S. degree in electrical engineering from UCLA in 2004.

As part of the funding program for her Ph.D. study, she was an intern at Texas Instruments in summers from 2004 to 2006, where she was involved in a pilot study to investigate the feasibility and limitations of traditional analog phase-locked loop architectures. During the internship, she has also completed the migration of a digital PLL design from 65nm to 45nm CMOS technology within a month.

Currently, her research interests include PLL/DLLs for on-chip clock generation, clock-and-data recovery, and high-speed links, especially focusing on the development of digital PLLs for nanometer-scale technologies.